

Triggers, data flow and the synchronization between the Auger surface detector and the AMIGA underground muon counters

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Abstract. The aim of the AMIGA project (Auger Muons and Infill for the Ground Array) is an investigation of Extensive Air Showers at energies lower than by standard Auger array, where the transition from galactic to extragalactic sources is expected. The Auger array is enlarged by a relatively small dedicated area of surface detectors with nearby buried underground muon counters at half or less the standard 1.5 km grid. Lowering the Auger energy threshold by more than one order of magnitude allows a precise measurement of the cosmic ray spectrum in the very interesting regions of the second knee and the ankle. The paper presents the working principle of the Master/Slave (standard Auger surface detector/the underground muon counters) synchronous data acquisition, general triggering and the extraction of data corresponding to the real events from underground storage buffers.

Keywords: AMIGA, trigger, FPGA.

I. INTRODUCTION

The Pierre Auger Observatory has been designed to study the highest-energy cosmic rays in nature ($E \geq 10^{18.5}$ eV). The determination of their arrival direction, energy, and composition is performed by the analysis of the atmospheric showers they produce. The Auger surface detector (SD) array consist of 1600 water Cherenkov detectors placed in an equilateral triangular grid of 1.5 km spacing [1].

AMIGA proposes to enhance the Auger acceptance at full efficiency down to 10^{17} eV by means of an SD graded infill deployed at smaller distances over an area much smaller than Auger. Trigger simulations show that grids of 433 m and 750 m detector spacing are fully efficient down to $0.35 \cdot 10^{17}$ eV and 10^{17} eV, respectively and therefore these geometries are being adopted. Areas of 5.9 and 23.5 km² will suffice to have a reasonable flux and they will require, apart from the Auger detectors at the 1.5 km spacing, an extra 24 and 42 ones, respectively. The infill SD stations are almost exactly the same Cherenkov detectors employed in the present Auger surface array, the only design parameters being changed are the spacing [2] and considered new 4th generation of the single chip Front-End (FE) providing the 80 MHz sampling (the same frequency as the global clock in the underground electronics) in comparison to the standard Auger, which works only with the 40 MHz sampling [3]. Data from underground muon detectors are formatted in

the 1st input routine in the FPGA according to the Figure 1 with the frequency of 320 MHz.

Each muon detector has an area of 30 m² and will be buried alongside each SD station at a depth of ca. 3 m. The distance to the station is large enough to avoid the water-tank shadow, guaranteeing a uniform shielding, but small enough to represent the same physical point inside the shower front and to be able to share GPS time signals and the micro-wave link with its associated surface detector. The relatively small distance allows the full synchronization of the surface and underground detectors by a triggering of the muon counters from the surface detector via dedicated fast transmission line.

II. TRIGGER/MEMORY SYSTEMS

64 analog channels (amplifiers, comparators etc - forming the signal from the PMT to the standard LVTTL level driving the FPGA inputs) are split on 8 daughter boards (see Fig.1 in [4]). Due to the optimization of the PCB, the part of the slow control functions has been moved from the microcontroller (μ C) to the FPGA.

In particular, 8-channel 12-bit DACs (TLV5630 by Texas Instruments) are controlled directly from the FPGA, where the SPI controller had to be additionally implemented. These DACs are located on each daughter board and they are driving the comparators to discriminate the proper level. Although the μ C contains 3 SPI controllers, routing lines from the μ C-board to the daughter boards were less optimized than those directly from the neighboring FPGA.

The underground electronics can work in two different modes:

- with the external trigger coming from the surface detector (synchronous mode) or
- with self-trigger generated from scintillator pulses (autonomous mode).

In the autonomous mode the trigger is generated directly from the 64 lines driven by the scintillators. An additional routine calculates a number of “fired” lines in a single time bin. If the amount of active lines is $\geq N$ = an arbitrary threshold (Occupancy) the final trigger is generated. This corresponds to a selection of any N-fold coincidence from 64 lines. The mode can be selected in any time from the CDAS.

In the synchronous mode the trigger has to be transmitted from the standard Auger detector to the underground electronics with a minimal delay, without

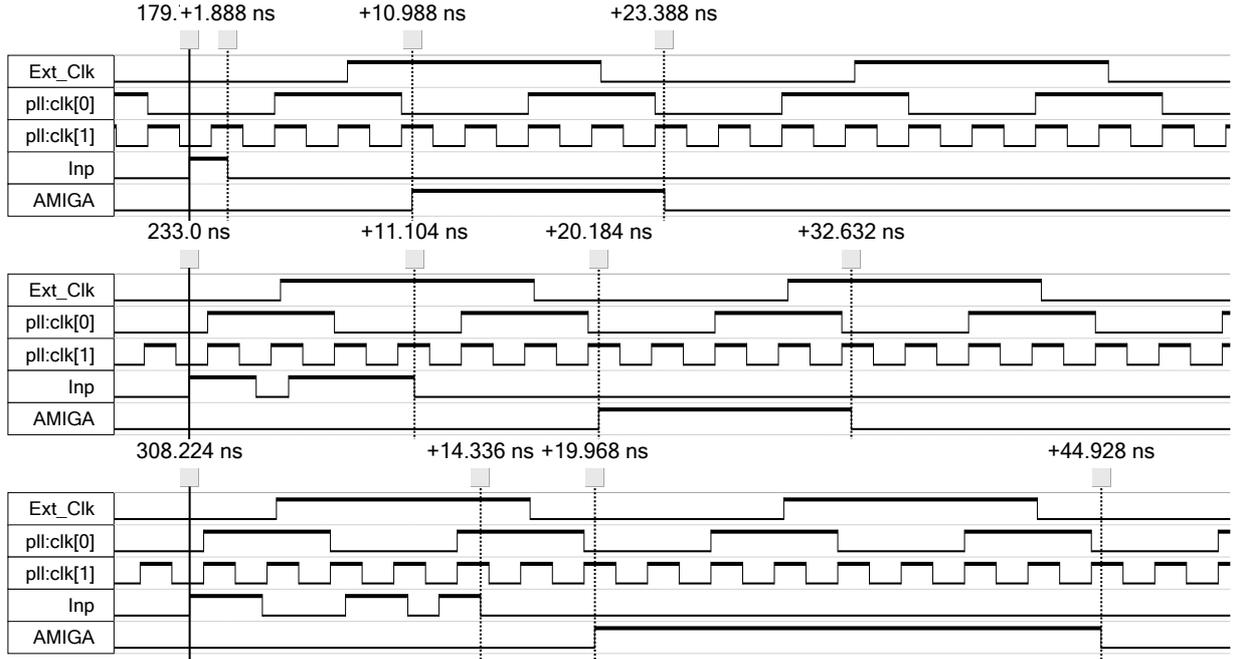


Fig. 1: Input pulses from the scintillator are sampled with 320 MHz clock (generated internally in the FPGA by the PLL circuit) and are enlarged to $N = \left\lceil \frac{n}{4} \right\rceil + 1$, where n - number of rising edges of the 320 MHz clock during the input pulse (including also gaps), N - number of rising edges of the global clock (80 MHz) during the output pulses. The “length” of output pulses = $N * 12.5$ ns.

a jitter and with correct sharpness of its rising edge. All these requirements can be accomplished only by a dedicated transmission line with a perfect adjustment of the wave impedance both: to transmitter driving the line and receiver resuming the signal. The distance between surface detector and the AMIGA scintillators does not exceed 15 m. The line consists of twisted-pair wires, and will transmit the trigger in a differential mode in order to suppress potential interferences on both wires. The additional source of the signal delay and possible jitter is the galvanic barrier, separating grounds between surface tank and underground electronics. Both grounds have to be separated in order to avoid loop currents. However, this requires the insertion of additional devices in both transmission chains: for the trigger and for the communication link between the underground microcontroller and the Surface Single Board Computer (SSBC). Preliminary measurements gave the average delay of 105 ns with a negligible $jitter_{p-p}$ (~ 55 ps) [4]. The barrier could not be built with opto-couplers; a sharply enough rising edge on the transferred signal cannot be assured even with the fastest ones.

The ADuM1100 - a digital isolator based on Analog Devices Inc. iCoupler[®] technology has been used. It merges high speed CMOS and monolithic air core transformer technology and provides outstanding performance characteristics superior to alternatives, such as opto-coupler devices. The ADuM1100UR supports data rates up to 100 Mbps. However, in order to achieve this data rate it has to be supplied by relatively high voltage +5 V unavailable on the PCB. The additional

+5 V required by linear regulator is provided by the ADM660, a charge-pump voltage converter that doubles the input voltage (standard +3.3 V).

In the synchronous mode data recorded in both surface and underground detectors are synchronized in that sense, that they correspond roughly to the same time window. A small phase shift is due to a propagation delay on the trigger transmission path. In order to provide a data synchronization, the surface detector firmware has been equipped additionally with the time stamps counter. The T1 trigger rate (the rate of events temporarily stored in the FPGA buffers in the surface detector trigger/memory system) is tuned in the calibrating process to ca. 100 Hz. All data relating to the T1 are transferred to the Unified Board (UB) and next investigated to look for a correlation with neighboring detectors in order to extract physics events (real showers). The searching process requires an extensively communication with the Central Data Acquisition System (CDAS). If a real shower appears and several tanks are hit simultaneously, the CDAS generates the T3 trigger and sends a request to all hit tanks for full data transmission. However, it takes even up to several seconds. In mean time data (shower profiles) are stored in the UB’s cache memory. Assuming maximal time 10 s and the average T1 trigger rate 100 Hz, the cache memory has to have a capacity to store 1000 event data. In order to recognize data corresponding to the T3 trigger among stored event in the cache memory, all event data are indexed by the time stamp counter. Shower profiles are registered in the time window of 19.2 μ s. Assuming 20-bit time stamp

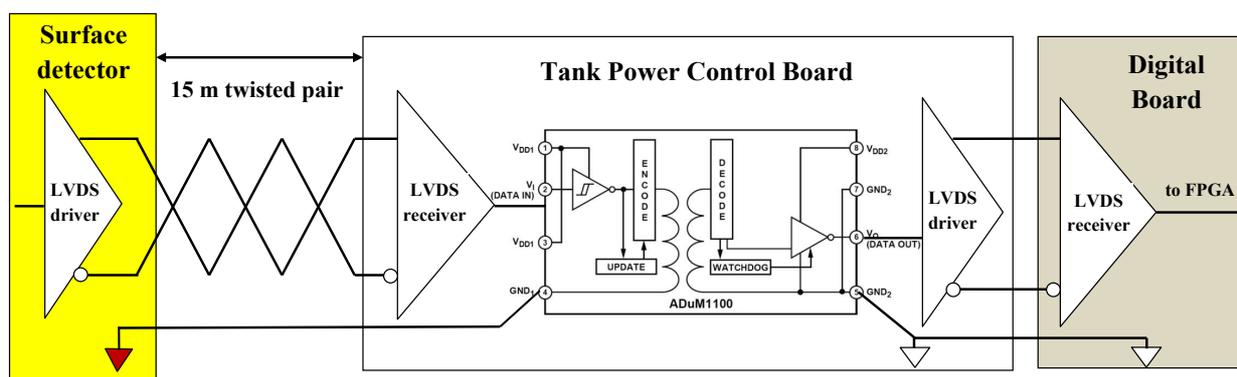


Fig. 2: The scheme of the dedicated transmission line for the trigger.

counter, the full time range of counting is ca. 20 s, long enough in order to avoid any misinterpretation. The time stamps from the event counter are transferred to the underground electronics just after the T1 trigger via the same dedicated transmission line. The protocol takes into account also a parity control. Time stamps are next stored in the internal memory of the FPGA.

A storage of 1024 scintillator events from 64 channels for 19.2 μ s by 80 MHz sampling and only 1-bit resolution requires 12 MB of memory. The selected FPGA does not contain such big internal memory. The system has to be supported by the external memory buffer. The external memory should be low-power type especially in the idle mode. Assuming full speed for writing (the same clock as for sampling), the write process of the single event would take only 19.2 μ s (in 64-bit data configuration). However, the T1 rate is only ca. 100 Hz, it means average interval between events is ca. 10 ms, 500 more longer than the writing process. Even if we decrease the writing clock to 10 MHz and use 32-bit bus, time needed to write a single event into the external memory is 307.5 μ s, still short in comparison to the T1 interval. It means the external memory works mostly in the idle mode. This condition practically eliminates Synchronous Static RAMs, because of huge power consumption, also in the idle mode. This type of memories is used mostly in very fast application, where a power budget is not a issue. Additionally these memories are really expensive and with relatively low capacity. The other option Synchronous Dynamic RAMs could be a good choice (only a single chip and still fully synchronous design), however the power consumption is still on relatively high level.

Finally, the Asynchronous Static RAM has been chosen. The CY62177DV30 is a high-performance CMOS static RAM organized as 2M words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular phones. The device also has an automatic power-down feature that significantly reduces power

consumption. Due to $19.2\mu\text{s}/12.5\text{ns} = 1536$ words of 64-bit data, we used 4 chips of ASRAM with 32-bit data bus and 4 194 304 depth, which corresponds to 22-bit address bus. The ASRAM CY62177DV30 works with only 10 MHz clock. The current consumption in the idle mode is only 1 μ A (in comparison to 120 mA of CMOS Standby Current for SSRAM like i.e. CY7C1486V25). An application of the SDRAM driven from the FPGA is keeping as an option, if the integrated PCB would require more space (1 SDRAM chip instead of 4 chips of ASRAM).

Triggered event from scintillators is temporarily buffered in the internal FPGA memory. 64 channels with 512+1024 time bins in investigated time window required by the AMIGA design correspond exactly to the same memory structure used in the surface detector trigger/memory system. Here 64 (1-bit) channels replace 6 (10-bit) FADC buses [5]. 2 bits on 32-bit data bus for AC/AF indices denoting circular or fixed buffers for high- or low-gain channels are used now for real scintillator channels. Data stored temporarily in the FPGA buffer internal memory, which correspond to the registered event triggered by the surface detector T1 trigger, are next transferred to the external memory with a large capacity. The time stamps are stored inside the FPGA. Two memory buffers working in the interlaced mode reduce a dead time of the system. When the 1st buffer is receiving data from the scintillators, the 2nd can independently transfer previously collected data into the external memory, working as a ring buffer. After ca. 10 s old data are being overwritten by the new one. The old ones are irrevocably lost. The system works in infinite loop. However, when the CDAS generates the T3 trigger, the SSBC sends via CAN BUS a request to the underground μ C asking to extract physics data related to the T3. The SSBC attaches to the T3 request also the corresponding time stamp.

The time stamp generated in the special counter in the Front-End FPGA of the surface detector is attached as the 762nd word on the tail of the trace of the high-gain channel. The SD firmware works in the diagnostic mode.

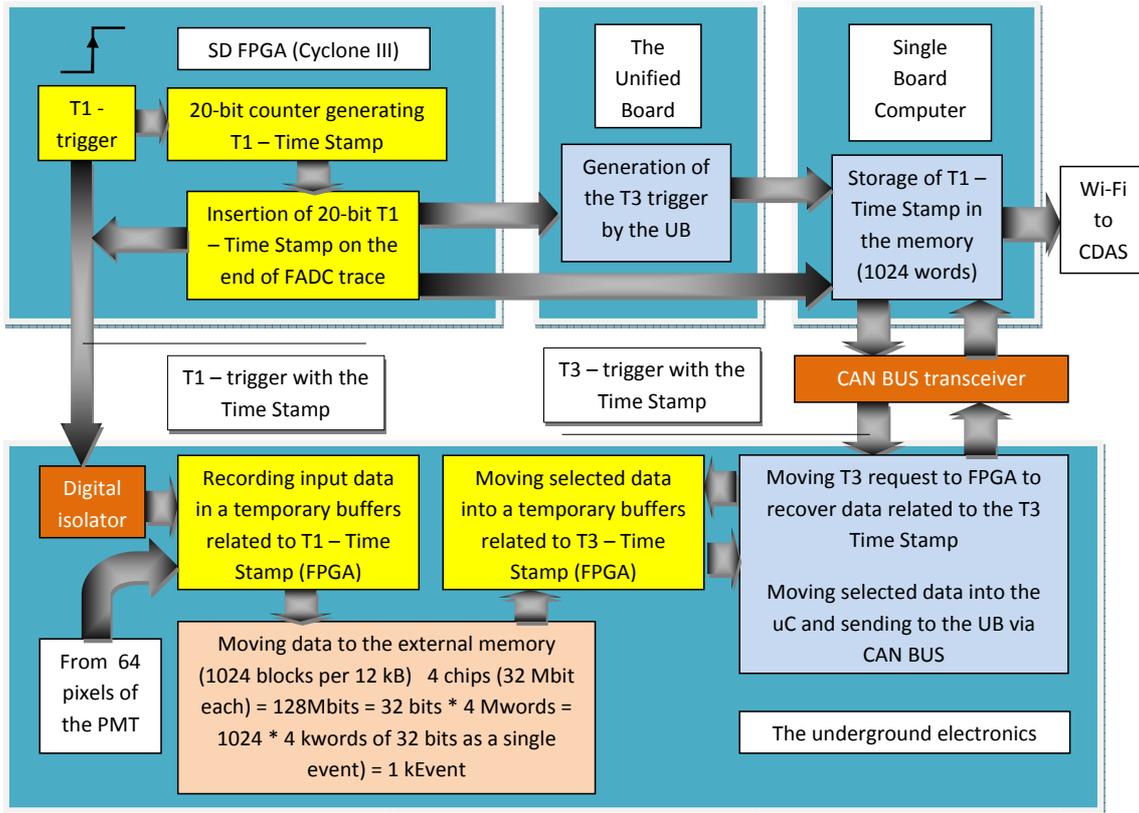


Fig. 3: The structure of the data flow and the synchronization of the underground electronics with the Auger surface detector.

The 762nd word was originally occupied by SDThr threshold in the slow channel, however it actually is not used and can be replaced by the AMIGA time stamp. Such an approach does not require a significant modification of the UB and the CDAS software. When the T3 trigger appears, the UB has to extract only a single word from the stored shower profile and send to the SSBC. When the time stamp achieves finally the FPGA via CAN BUS and the underground μC , it is used to generate the address of the event stored in the external memory. The best tool would be the Content Addressable Memory (CAM). Unfortunately, the CycloneIIITM family does not support the CAM mega-function. It is available only in obsolete APEX families. The routine generating the address has to use the standard comparison mechanism word by word. For the depth of the time stamp memory of 1024 words, it takes maximal 12.8 μs . The T3 rate is on the level of minutes. Also 10 s storage interval gives a sufficient safety margin. The probability that data cannot be extracted from the RAM due to additional searching procedure is negligible. The address associated to the time stamp allows extraction of data from the external memory. It appears without any synchronization with the writing process of scintillator data. In order not to interrupt the data transfer from the FPGA to the external memory, when the event address is ready, the FPGA sets a flag blocking the next data transfer. When the current

transfer expires, the FPGA starts the reverse process, reading data from the external RAM and transferring to the internal memory buffer - FIFO. Because of the same clock, the reading process takes exactly 307.5 μs . When the FIFO is full, the FPGA automatically changes a direction of the data transfer, from the FPGA to the ASRAM. Data from the FIFO are available for the μC and they are next transmitted via CAN BUS to the SSBC and finally via a radio link using the IEEE 802.15.4 standard to the CDAS (Figure 3).

III. SUMMARY

The full data path transfer (trigger procedures, internal buffers, writing data to the external ASRAM, reading data from the ASRAM to the internal FIFO in the FPGA, transfer data to the μC and next via CAN BUS to the SSBC) has been successfully tested. The optimization of the system performance is in progress.

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