Nuclear Instruments and Methods in Physics Research A 606 (2009) 439–445

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

The 3rd generation Front-End cards of the Pierre Auger surface detectors: Test results and performance in the field

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ARTICLE INFO

Article history:
Received 9 March 2009
Received in revised form
21 May 2009
Accepted 22 May 2009
Available online 13 June 2009

Keywords:
Front-End
FPGA
Cyclone
Pierre Auger Observatory

ABSTRACT

The surface detector array of the Pierre Auger Observatory comprises 1600 water Cherenkov detectors distributed over an area of 3000 km^2. The Cherenkov light is detected by three 9-in. photo-multiplier tubes from which the signals of the anode and last dynode are digitized by 10 bit 40 MHz FADCs. An Altera Cyclone FPGA is employed to generate different local triggers and to handle the data transfer to a communication board. After briefly discussing the design of the cards we present an autonomous test-bench, which has been set up in order to test the large number of boards prior to installation in the field. The qualification procedure and the results obtained in the laboratory are presented. Up to three years of operation in the field demonstrate a very good performance and reliability of the Front-End cards.

1. Introduction

The Pierre Auger Observatory is located in the Province of Mendoza (Argentina) and it aims at measuring cosmic rays at the highest energies with unprecedented statistics and resolution. To fulfill these goals, it comprises two major components: 1600 water Cherenkov detector stations distributed over an area of 3000 km^2 for measuring the charged particles associated with extensive air showers (EAS) and 24 telescopes with 30×30 degrees field of view and 12 m^2 mirror area each to observe the fluorescence light produced by the charged particles in the EAS during operation in clear moonless nights. The simultaneous observation of EAS by the ground array and the fluorescence light is called "hybrid"-observation. It improves the resolution of the reconstruction considerably and, due to the calorimetric nature of the emitted fluorescence light, provides energy measurements virtually independent from hadronic interaction models used to model EAS [1].

2. Design of the SD front electronic boards

Three 9-in. photo-multiplier tubes (PMTs) read out the Cherenkov light from the 120 00 l of purified water contained in each tank. The signals from the anodes (low-gain channel) and dynodes (high-gain channel) are transported on equal-length shielded cables to the Front-End Board (FEB), attached as a daughter board to a Unified Board (UB). The UB contains a microcontroller that manages all processes related to the data acquisition in the detector station.

The splitting of the signals allows an extension of the dynamic range of the measured energy range to 15 bits with 5 bits overlapping. The system digitizes the six analog signals of each detector station in the multistage differential pipeline architecture AD9203 analog-to-digital converter (ADC) at 40 MHz. Signal filtering is performed by anti-aliasing 5-pole Bessel filters with 20 MHz cut-off. The outputs of the six 10-bit ADCs are processed by an Altera® Cyclone™ FPGA [2] working at 300 MB/s as trigger/memory circuitry (TMC) supported additionally by a Dual-Port RAM memory as a temporary buffer.

The AD9203 is specified to work correctly over the full operating temperature range from −20 to +70 °C. The TMC evaluates the ADC outputs for interesting trigger patterns, stores the data in a buffer memory, and informs the UB in case a trigger occurs. The UB sends short trigger packets and, when requested, full event data to the observatory campus via a wireless network. A structural diagram of the FEB is shown in Fig. 1.

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doi:10.1016/j.nima.2009.05.163

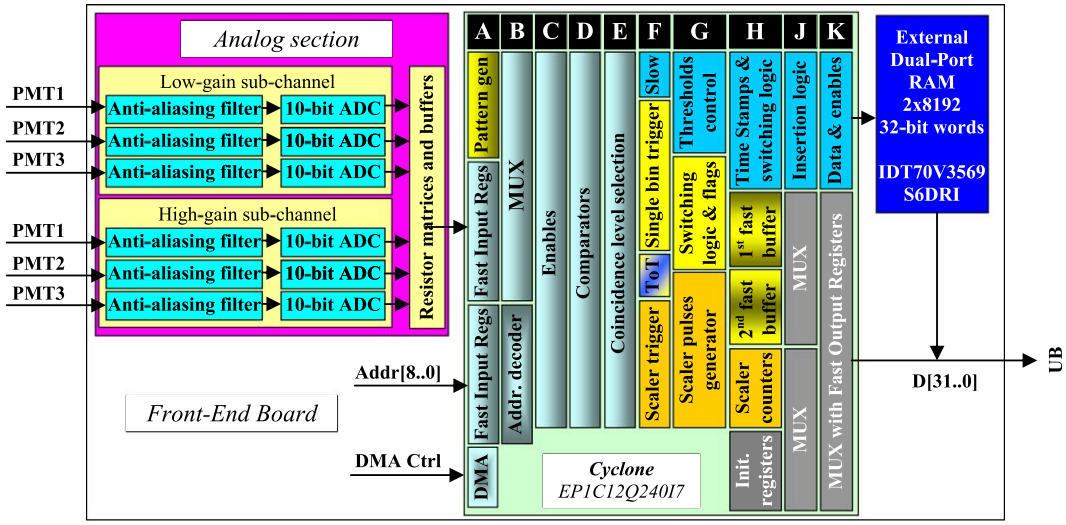

Fig. 1. Structure of the Front-End Board. Three high-gain and three low-gain channels amplify and shape the analog signals from three PMTs (anode and dynode) in 5-pole Bessel anti-aliasing filters. The shaped signals are digitized in six ADCs and further processing is performed in the Cyclone™ FPGA. All processes are split into sub-processes performed in the single clock cycle and encapsulated in the A,B,C,... procedures.

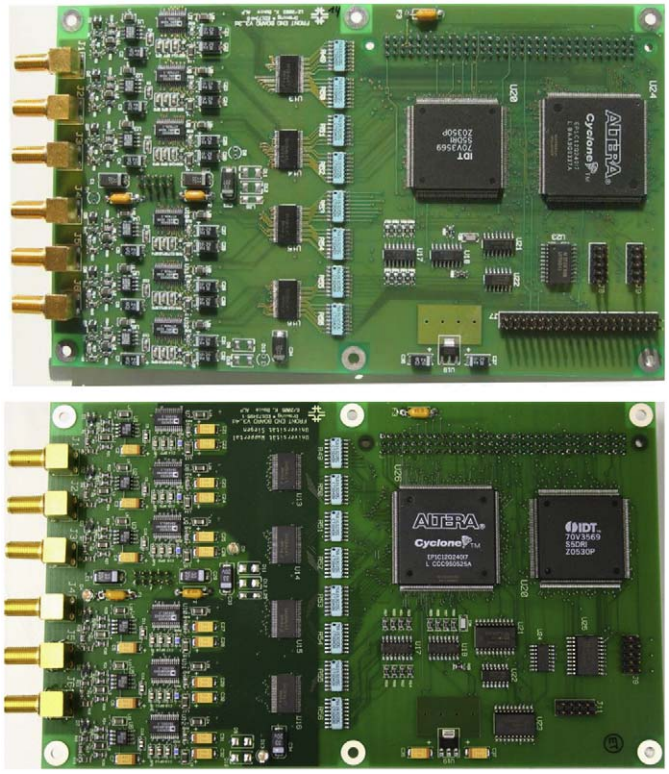

Fig. 2. The Cyclone™ 3rd generation prototype (top) and production (bottom) Front-End Board.

The funding flow dictated that the FEBs were made in two distinct batches, with the second batch occurring several years after the design of the first batch had been frozen. This allowed design changes to be incorporated in the FEB to take advantage of newer FPGA chips, both reducing the cost and improving the performance of the boards.

The first batch of FEBs used two Altera® ACEX® family PLDs. This board which in the Auger history is of the 2nd generation, and its test system is described in Refs. [3,4].

The second batch of FEBs (i.e. the 3rd generation) replaced the two ACEX® PLDs with a single Altera® Cyclone™ FPGA. This allowed a significant simplification of the board layout, a simplification of the trigger software because it avoids problems with chip synchronization (see Ref. [5]), it reduces the power consumption as the core is supplied by 1.5 V only, and it reduced the total costs. Moreover, the Cyclone™ chips contain much more internal memory avoiding the need to support the TMC by external memory. Nevertheless, to minimize modifications, the external larger memory was kept rather than occupying internal memory blocks. This also allows implementing more sophisticated trigger conditions as part of possible future upgrades [6].

However, to improve the signal routing and to reduce the noise level in the analog part of the board, the location of the FPGA and memory chips has been swapped with respect to the previous generation of Front-End cards. Fig. 2 presents the prototype version (top) and final layout (bottom) of the 3rd generation FEBs. The test system for this generation is described below.

3. Quality parameters to be tested and impact on physics results

The test set-up was required to perform full tests of the following parameters in each channel:

1. full verification of digital data flow,
2. integral and differential non-linearities of the analog section and ADCs,
3. cut-off frequency of the anti-aliasing filter, and
4. pedestal and noise of the analog section.

The full verification of digital data flow from the digital inputs, through the trigger system, internal memory buffer and the DMA transfer from the FPGA to the UB for both the fast and the slow channel—through the trigger system, the logic circuit inserting time stamps, the external memory and finally also the DMA transfer from the Dual-Port RAM to the UB—is a first test to verify that no line is shorted or broken. Also, the identification of any

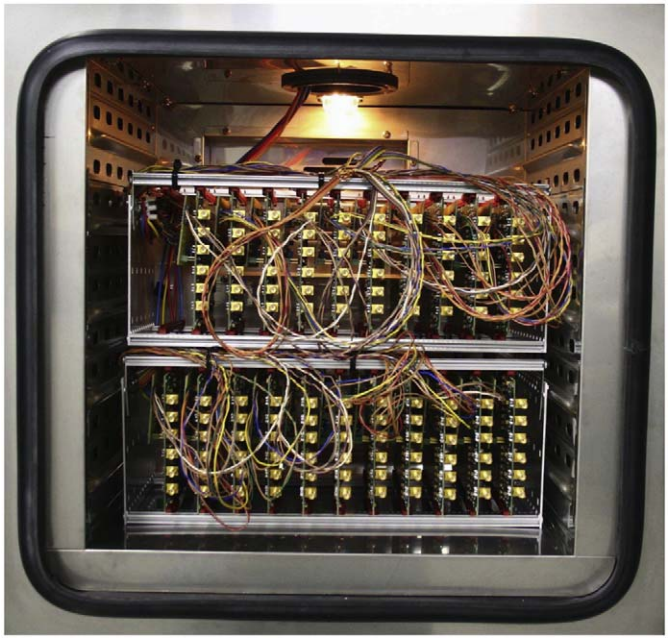

Fig. 3. Up to 22 FEBs were placed in a climate chamber for burn-in under electric power.

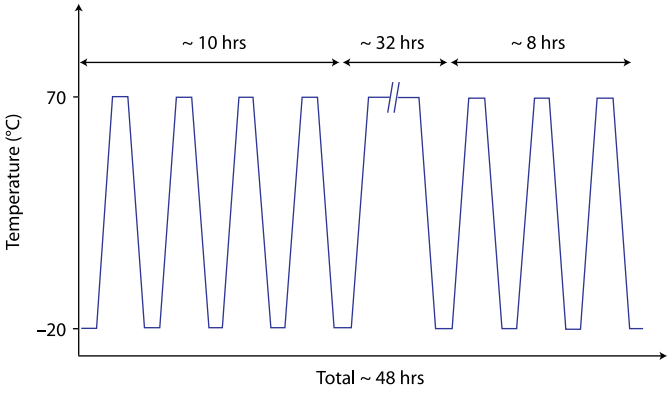

Fig. 4. The temperature profile for the "burn-in" test.

corrupted bit on the full data flow path is to be provided by the test bench.

The integral non-linearity of the ADC is crucial to assure a linear correspondence of the analog signals to the digitized values. Accepted errors of the analog-to-digital conversion may come only from the quantization process. Differential non-linearities, on the other hand, are particularly disturbing for small signals as they deteriorate the resolution and could significantly affect the Time-over-Threshold (ToT) trigger rate.

The cut-off frequency according to the Nyquist theorem should be 20 MHz. Due to aliasing, too large values may violate the integral linearity of the analog section. Too small values, on the other hand, reduce the capabilities to analyze the rise time of the signals and thereby degrade the sensitivity to the cosmic ray composition and to the detection of neutrinos in highly inclined EAS. Moreover, a smoothed falling edge enlarges the tail of the signal and affects ToT-rate. A ToT trigger is generated if within a sliding window of 120 consecutive time bins at least 12 or more samples are above a relatively low threshold (30% of the equivalent light produced by a vertical throughgoing muon). Thus, an enlarged tail of the signal artificially increases the number of "fired" bins and spuriously increases the ToT rate.

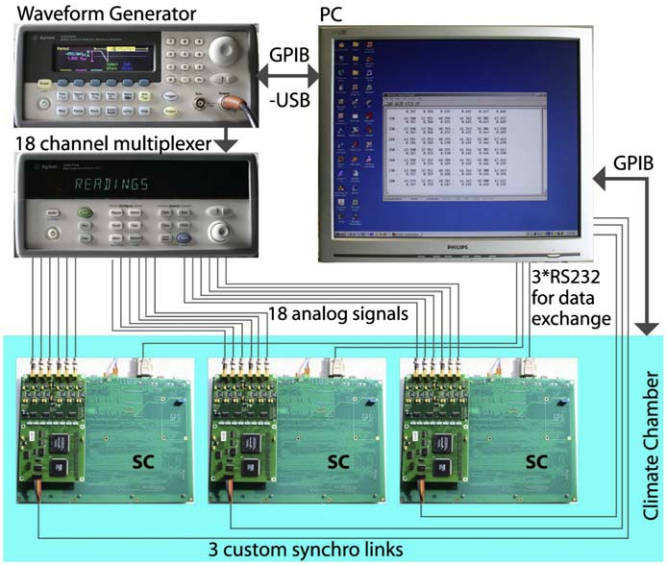

Fig. 5. Sketch of the automized test system.

The ADC pedestal should be in a range of 20–80 ADC-channels. Too high pedestals reduce the dynamic range and too low ones disable the analysis of undershoots observed after very large pulses. Due to the low thresholds for the triggers, too large noise levels need to be avoided as much as possible.

4. Test set-up

Prior to the production of the new Cyclone generation of 800 FEBs at an outside company [7], 10 units were manufactured in a preproduction batch to verify the new design [6]. The boards were tested intensively at room temperature and in extreme conditions in the climate chamber. No malfunctions were observed. In order to perform the acceptance tests of the full batch within a time period of about half a year, a highly automized test bench has been developed and installed in the laboratories at each University.

All the boards had to pass the following tests:

(1) The boards were powered up and the current in the digital and analog part was verified to be in the specified range. All manufactured boards passed this initial test.
(2) Next, groups of up to 22 current supplied boards were placed into a climate chamber (Fig. 3) while a "burn-in" test was performed for 55 h (Fig. 4). The test started with four thermal cycles between +70 and −20 °C over a period of 10 h, followed by a 35 h "burn-in" period at +70 °C followed again by 10 h with four cycles between +70 and −20 °C. Formation of dew during temperature cycling was avoided by enriching the atmosphere in the climate chamber with Nitrogen.

A sketch of the hardware test configuration is depicted in Fig. 5. A waveform generator provided pulses of various forms to a high quality 3 × 6 channel multiplexer. The 18 outputs were fed into three FEBs for simultaneous testing. Each of the multiplexer outputs could be switched on/off individually via a GPIB interface so that each FEB channel could be tested individually and crosstalk tests be performed. The data of the FEBs were read out via the Pierre Auger surface detector UB. In the lab, the data were

transmitted via an extra RS232 interface (integrated on the UB), instead of the microwave link used in the field.

The RS232 interface was also used for uploading the firmware into the UB after powering up. The FEBs were controlled via custom made synchro opto-coupled links using the parallel-port interface of the PC and the I^2C protocol for data exchange. The PC also controlled the waveform generator, the multiplexer, and the climate chamber, so that the full sequence of acceptance tests could be programmed and run in an automized mode.

For three simultaneously tested boards, the full sequence of tests (at −20, +25 and +70 °C) and the data transfer and storage on the PC lasted about 4 h. Most of the time was actually needed for changing the temperature in the climate chamber. In this way, up to nine FEBs could be tested per day.

5. Digital tests

The communication with all registers of the FPGA chip in the FEB is verified by writing and reading several tens of random numbers per address. The FPGA chip is programmed correctly if the read data are matched by a pattern of written random values. No mismatch is tolerated.

For diagnostics, several test routines have been implemented additionally into the FPGA code. The first pipeline stage of the code could work as DAQ or as an internal pattern (“event:” or “noise”) generator.

The “event” generator is sending 10 pulses (on ADC[29..20] the sequence is #3FF, 0, #3FFh, ..., 0, #3FF) and afterwards a pulse (#3FF) each Div1*Div2 (μs). The bus ADC[9..0] is increasing/decreasing continuously with the clock cycle; bus ADC[19..10] is decreasing/increasing, respectively. The sum of both busses ADC[19..10] + ADC[9..0] is constant = #3FF. The “event” generator is controlled by two 12-bit words treated as dividers of the main clock. The global 40 MHz clock is divided preliminary by a factor of 40–1 MHz and afterwards is divided again by a product of Div[23..12]*Div[11..0]. With that frequency the ADC[29..20] bus is toggled on/off from zero to the saturation state. This generator was used to measure the current consumption for the I/O and the core of the FPGA vs. the trigger rate.

The “noise” generator produces a pseudo-random signal to verify the behavior of the system. We then investigated possible correlations between the busses and checked the structure of consecutive DMA transfers, to identify reminiscence patterns of a previous DMA transfer.

For this purpose, the “noise” generator mixes up all bits in the two 10-bit up and down counters and performs an additional Ex-OR with 30 bits of the pattern register. The patterns in consecutive DMA transfers were changed by additional mixing of the bits with the counter of the DMA transfers. This was independently done for the fast and slow channels. The “noise” patterns obtained in simulations are then used for online comparison with the pattern obtained from the real internal generator implemented inside the FPGA. Due to limited memory space in the UB, the patterns for the fast and slow channels were limited to 768 and 512 kB, respectively. They correspond to 128 DMA transfers for the fast channel (6 kB = 768 words of 60 bits) and 64 DMA transfers for the slow one (8 kB = 2048 words of 30 bits).

The artificial data from generator are read out just like real ADC data. They pass through all trigger/memory processes and they are finally sent to the UB, where they are compared to the simulated patterns. Moreover, the internal counters are synchronized with the DMA transfers to provide proper patterns for the comparisons. These tests were performed as the first ones at each temperature, before checking the analog section of the FEB.

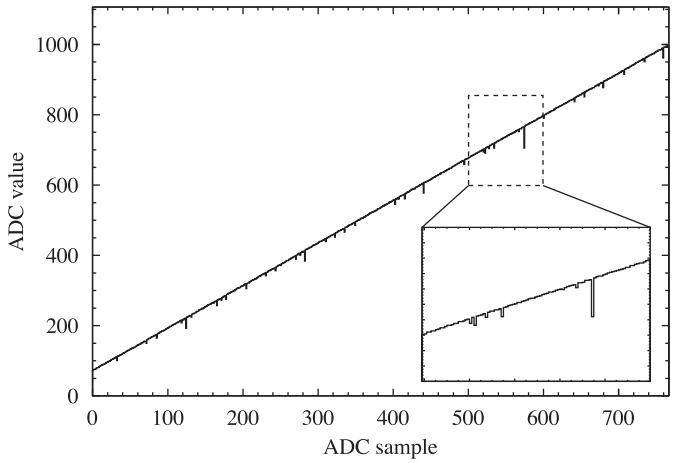

Fig. 6. Artificial non-linearity due to a jitter of data outgoing from the FADC.

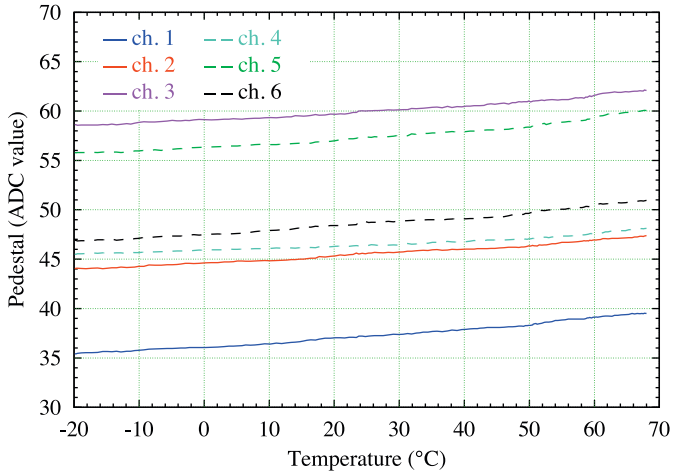

Fig. 7. Pedestals (in ADC-counts) for the six channels of an individual FEB as a function of temperature.

6. Integral and differential non-linearity, and timing optimization

The integral and the differential non-linearity were tested by ramping up the input signals using a saw-tooth waveform and analyzing the digitized signals as a function of time (sample number). The rising edge of the analog signal was 19.2 μs, corresponding to the 768 word length of the fast buffer which registers the shower profile. For the integral linearity the correlation coefficients (CC) were calculated for all 768 words. The values of $(1 - CC)$ were typically a few times 10^{-6}, slightly above the minimal value originating from the quantization of the analog signal in the ADC. The correlation between the ADC-counts in consecutive time bins allows also finding suspicious transitions, which correspond to the possible differential non-linearities.

For this purpose, measurements with ramped up signals were repeated 64 times and the deviation of the measured and expected ADC value in each of the 768 samples was filled into a histogram. In case the standard deviation integrated over the full ADC range exceeded 0.95 ADC channels, the board has been rejected.

Preliminary tests showed ca. 10% of channels in FEBs with suspicious structures in the linearity graphs (see Fig. 6), but only

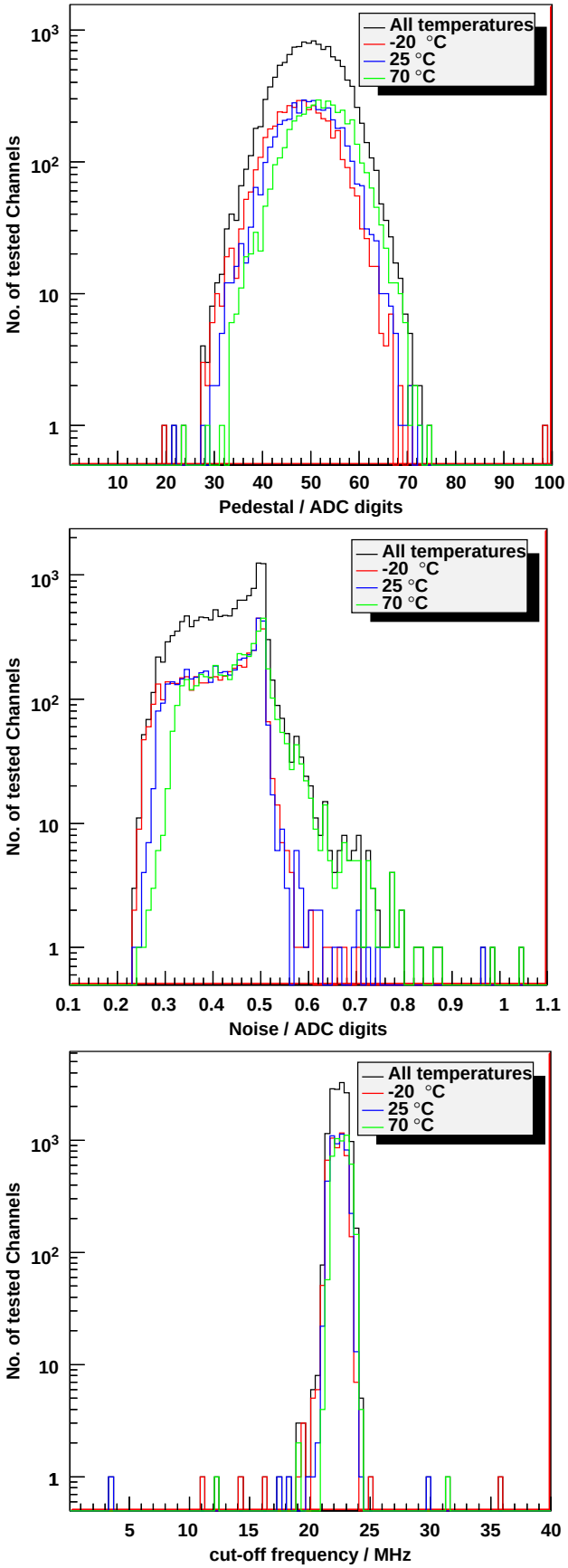

Fig. 8. Pedestals, noise and cut-off frequencies vs. temperature as measured in the lab.

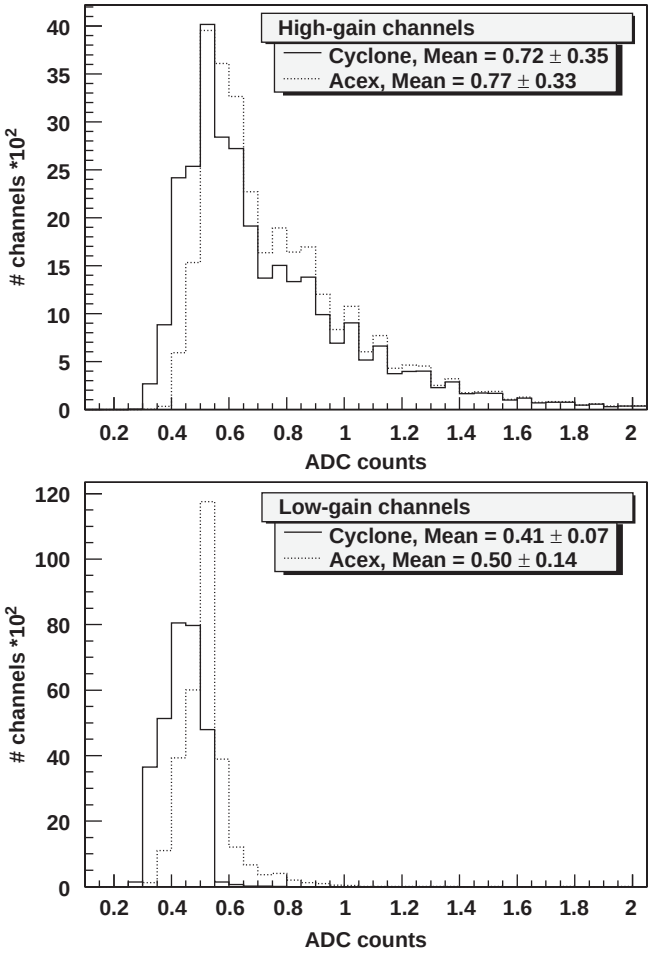

Fig. 9. Comparison of the noise levels for the high- (top) and low-gain channel (bottom) for the Cyclone and ACEX FEBs measured in April 2008, for 175 386 events registered in Cyclone FEBs and 324 035 events registered in ACEX FEBs. In field conditions $\sigma_{Cyclone}^{high-gain} = 0.72$, while $\sigma_{ACEX}^{high-gain} = 0.77$ and $\sigma_{Cyclone}^{low-gain} = 0.41$, while $\sigma_{ACEX}^{low-gain} = 0.50$. The graphs are normalized to the amount of events.

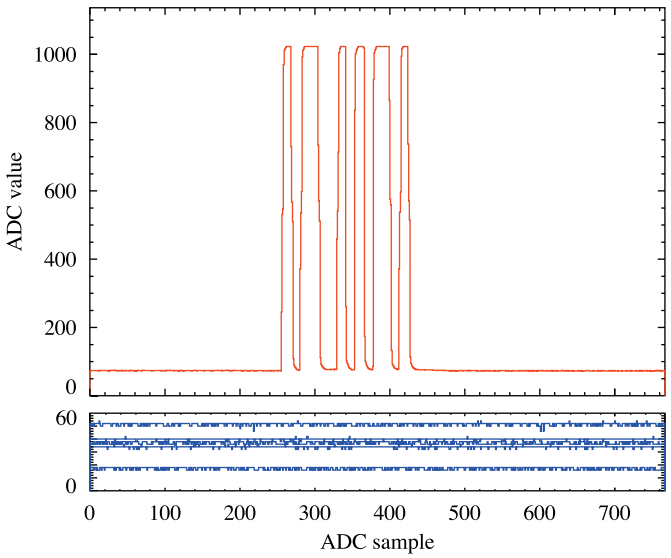

Fig. 10. A test pulse driving a reference channel. The oscillation from the pedestal up to the saturation is constrained between the 256th and the 429th time bin (with 25 ns grid) (above). No crosstalk is observed (bottom). The neighboring channels are running with the floating, not connected inputs.

at −20 °C. This apparent, differential non-linearity was in fact a result of a violation of the FADC data latching in the first stage of the FPGA pipeline. Although the temperature −20 °C is never supposed to be reached, the PLL condition has been modified to enlarge the reliability of the system.

Originally, the DMA transfer has been optimized to reach a maximal stable area for the transmitted data. The data are transferred from the FPGA into the DRAM in the Unified Board by the falling edge of the μC DMA signal (∼CAS3) edge. The internal PLL clock has been adjusted to locate this edge in the middle of the stable output data. However, this reduced the safety margin for the stable input data latched in the Fast Input FPGA Registers. Finally, a proper compromise between antagonistic requirements gave satisfactory results.

In total, only 6 of the 800 tested FEBs were rejected by the acceptance tests, due to their real differential non-linearities.

7. Pedestal and noise

The ADC noise and the pedestal are found to have a weak temperature dependence. Fig. 7 shows as an example the scattering of the pedestals in the six ADC channels of a single FEB and its weak increase with temperate. The effect of increasing pedestal with increasing temperature to air shower triggers is discussed in Ref. [8]. The distribution of the ADC pedestals and noise values of all tested boards and for each temperature is shown in Fig. 8.

The FEBs had to pass the following acceptance tests for each of the three temperatures:

1. ADC noise $\sigma_n < 0.8$ and
2. ADC pedestal between 20 and 80 channels.

As can be seen, the selection criteria are easily met by the boards, only at the highest temperature of 70 °C, some channels show a higher noise value.

As discussed above, the location of the Cyclone® chip and Dual-Port RAM on the PCB has been swapped with respect to the previous ACEX-based generation of FEBs to reduce the length of the connection lines. This modification was expected to suppress both the digital noise and the crosstalk. The result based on data obtained during operation in the field is shown in Fig. 9. Here, we compare the noise level of the 595 FEBs equipped with Cyclone chips that have been installed until April 2009 with the ones from the ACEX boards. The noise level in the ACEX compared to the Cyclone boards is found to be higher by 5.6% for the high-gain channel and by 21% for the low-gain one.

8. Crosstalk

The crosstalk was measured by injecting fast oscillating signals (see Fig. 10) at the saturation level to each channel and verifying the absence of crosstalk into the other channels. The signal in the time bins $(0,\ldots,255)$ and $(430,\ldots,767)$ in the investigated channels was taken as a reference value. If for time bins $(256,\ldots,429)$, when in the reference channel oscillations appear, the averaged level in investigated channels increased more than 0.2 ADC-counts, the channel was considered suspicious, with a potential crosstalk danger. Only two boards did not pass this test.

9. Cut-off frequency

The 5-pole Bessel anti-aliasing filter in the analog part has been designed to the 20 MHz cut-off frequency according to Nyquist requirements. The correct value of the cut-off frequency is important especially for Time-over-Threshold trigger. Too low cut-off frequencies cause a softening of the signals and an artificial increase of the ToT rate, while too high values may create problems due to aliasing.

The cut-off frequency was measured by injecting harmonic waves of 100 kHz, 18 MHz, 25 MHz and 30 MHz to the FEBs and analyzing the suppression of the digitized signals. The amplitude of the signals was extracted from the sine shapes, which were recovered by the least squares method. The cut-off frequency was defined by calculating the value at which −3 dB suppression was reached. The damping of the signals in the multiplexer and the signal cables themselves were measured independently and corrected for. Coaxial cables supplying the FEBs from the generator sometimes had to be replaced due to temperature material fatigue. Thus, the suppression coefficients for new cables had to be measured again. Due to the very wide bandwidth of the multiplexer (more than 2 GHz) the influence on the signal transmission was negligible.

The results are shown in Fig. 8. The majority of the FEBs shows cut-off frequencies in the expected range, between 20 and 25 MHz.

10. Final acceptance results

In total, 29 of the 800 tested FEBs were rejected by the acceptance tests because of their ADC pedestal (2) or noise (7), differential non-linearities (6), integral non-linearities (4), cut-off frequencies (6), non-working ADCs (2), crosstalk (2), problems in programming of the boards or due to wrong communication with registers (4). Some of these boards did not pass several tests.

Finally, accepted boards were coated with humidity sealer and shipped to the experimental site for installation. The results of the individual tests are compiled in a MySQL database and a graphical web-based interface is provided to make the data available to the collaboration and for future verifications [9].

11. Summary and conclusions

More than 800 readout boards of the Pierre Auger surface detector array have been produced and tested. This 3rd generation board has identical functionality as the previous generation, but could be produced at lower cost and with a simplified layout due to the usage of a more powerful Cyclone FPGA and it has a reduced power consumption and lower noise level in the ADCs. Prior to installation in the field all boards were investigated in the fully automatic test system allowing to test nine boards per day. About 3% of the FEBs failed in the acceptance tests. Some of them could be repaired by substituting individual components. The excellent performance of more than 600 FEBs operating in the field for up to three years by now confirms the high quality of the design and hardware.

Acknowledgments

We kindly acknowledge fruitful discussions and the cooperation with our colleagues in the Pierre Auger Collaboration, especially D. Nitz. Financial support by the German Ministry for Research and Education (BMBF) under Grants 05 CU5PX1/6 and

05 CU5PS1/1 is gratefully acknowledged. Part of this work was also funded by the Polish Committee of Science under KBN Grant no. 2 P03D 001 24.

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