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Implementation of the first level surface detector trigger for the Pierre Auger Observatory Engineering Array ☆

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Abstract

The Pierre Auger Observatory studies ultra-high energy cosmic rays in the range of 10^{18} eV up to the highest energies. The apparatus reaches full sensitivity above 10^{19} ev. The southern hemisphere site is currently under construction. When completed, the surface array at this site will contain 1600 water Cherenkov detector stations distributed over 3000 km^2. Prior to proceeding with full-scale construction, a prototype "Engineering Array", consisting of 40 detector stations was tested. This paper describes the implementation of the first level surface detector trigger used in the engineering array.

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Keywords: Pierre Auger Observatory; PLD; Triggers; Surface Detector Electronics

1. Introduction

The Pierre Auger Cosmic Ray Observatory [1] is designed to study the highest energy cosmic rays. The southern hemisphere site, when completed, will contain 1600 surface detectors and 24 fluorescence detector telescopes installed in 4 optical station buildings, each containing 6 telescopes. Prior to proceeding with construction of the full array, a small segment, called the Engineering Array (EA), consisting of nominally 40 surface detector stations and two fluorescence telescopes, was constructed to validate the design [2]. This paper describes the implementation of the first level surface detector trigger in the EA.

Each surface array station consists of a solar powered water Cherenkov detector, instrumented with low-power electronics that communicate with

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the observatory campus via a custom radio network [3]. Low gain and high gain (32 times larger) signals from three downward facing 9″ photomultiplier tubes (PMTs) are sent to the front end electronics, which conditions the signals before digitizing them. Every 25 ns, the outputs of six 10-bit analog to digital converters (ADCs) are presented to the trigger/memory circuitry. The trigger/memory circuit evaluates ADC outputs for interesting trigger patterns, stores the data in buffer memory and informs the detector station micro-controller when a trigger occurs. The station controller sends trigger packets, and when requested, event data to the observatory campus via a wireless network. A hierarchical event trigger is used to select events of interest and reject uninteresting events, while keeping within the rate constraints imposed by the station micro-controller, the communication link bandwidth and the central data acquisition system. The trigger/memory circuit generates the first of the hierarchical trigger levels [4–6].

2. Requirements

Cosmic ray showers passing through the water tank generate Cherenkov photons, which are detected by 3 PMTs. The main contribution to the signal comes from the electron, positron and muon components of the shower. The amplitude and time characteristics of the signals (rise and decay time) depend on the type of particle, the energy and inclination of showers, as well as the distance from the shower core.

The high and low gain signals from each of the three PMTs are digitized in two 10-bit ADCs and then sent to the trigger circuitry. Thereby, the covered dynamic range is 15 bits. The global (sampling and data processing) clock is 40 MHz.

The physics requirements manifest themselves in several general design requirements: (1) the circuit should record in the order of 20 ms of information for each event; (2) the outputs of six 10-bit ADCs must be recorded over this time span and (3) additional information should be continuously recorded for calibration purposes. Requirements (1) and (2) imply a memory 512–1024 words deep, and 60 (or more) bits wide. Requirement (3) can be satisfied with 30-bit wide memory, but requires kilowords of depth in conjunction with zero-suppression.

3. Implementation overview

The trigger circuitry is situated between the ADCs and the station micro-controller in the signal processing chain.

Several options were studied for implementing the trigger circuitry. A survey of components at the time identified PLDs which could satisfy requirements (1) and (2) by utilizing their internal memory. However, an external memory chip was required to satisfy requirement (3).

In the EA the choice was made to implement the trigger/memory circuitry using a programmable logic device (PLD) and a static RAM chip. The focus was to minimize the chip count and facilitate rapid algorithm development. Cost was a secondary concern. Cost optimization was postponed until the transition to the production design.

We chose to use the Altera APEX family EP20k200RI240-2 PLD chip [7], and an IDT 70V3569S6DRI 16k word by 36-bit wide dual port static RAM. The RAM chip easily exceeded our requirements. A 32-bit wide 8k word dual port static RAM chip would have sufficed, but none was identified. The PLD contained 52 256-byte memory blocks, sufficient to implement two 64-bit wide 768 word long event memory buffers.

The trigger circuitry was implemented on a small daughter board, which attached to a front-end board containing the analog signal processing electronics. The front-end board, in turn, attached to the station controller bus. An IBM PowerPC 403GCX micro-controller, with a 40 MHz external bus speed, supplied the processing power for the station. This high modularity was effective in the EA, as it facilitated the distribution of development work among several universities and laboratories.

The organization of the trigger board is shown in Fig. 1. A photograph of the board is shown in Fig. 2.

4. Code functionality

A basic set of features was selected to implement in the EA trigger; they are described in the following sections.

4.1. Event generators

Built-in self test (BIST) was incorporated in the trigger/memory circuit design from the outset. However, rather than using JTAG, with the associated overhead of additional test circuitry, we opted instead to implement BIST using internal generators to test functionality in the absence of ADC inputs, and register read-back to test the bus interfaces. Moreover, as this was the first version of the trigger/memory installed in the field, we opted to be conservative in our event generator, implementing a wide variety of test input options.

These included a trigger generator, which generated triggers at specified intervals in order to verify the response of the system at various event rates and measure power consumption as a function of trigger rate. Sawtooth waveforms and pseudo-random noise-like patterns were implemented to check the trigger circuits. The latter was used in conjunction with a PC-based program, which predicted the PLD trigger and compared the waveforms read out with what was expected.

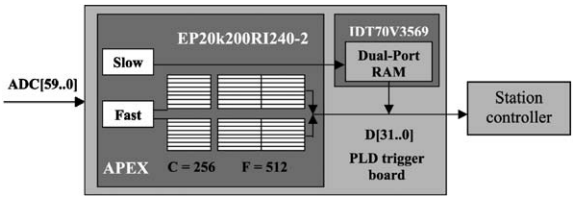

Fig. 1. A block diagram of the trigger board with the structure of an internal and an external memory.

4.2. Shower memory

The waveforms generated by extensive cosmic ray air showers are recorded in a shower memory. The shower memory acts like a digital scope, in which the signals before and after a trigger point

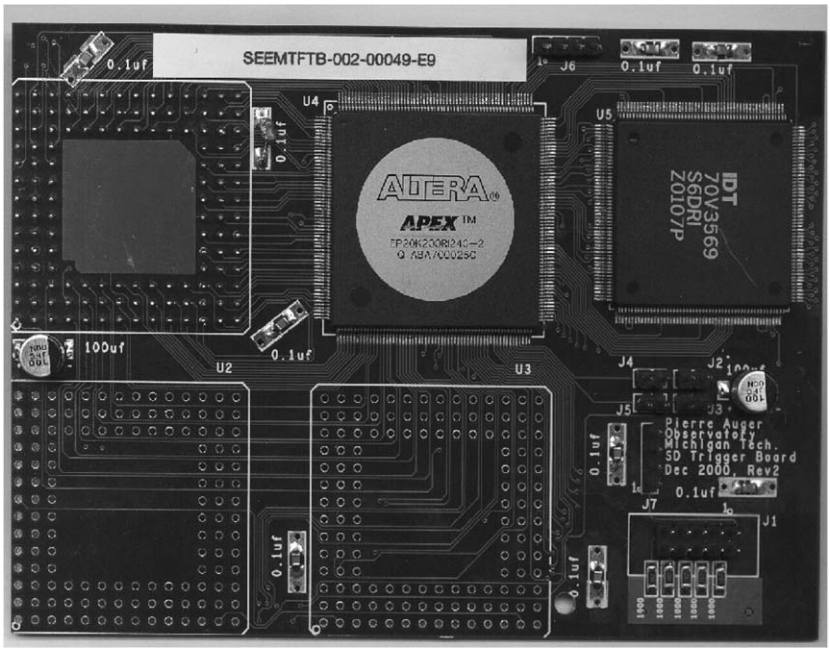

Fig. 2. Photograph of a trigger board used in the EA. In the upper left corner there is a plug to connect to the front-end board. The lower right corner contains a connector to an external PLD programmer. The two empty PGA132 packages were provided to test an alternative implementation using an ASIC.

are recorded. This memory is double buffered to minimize system dead time.

The most natural structure would have been to implement the shower memories as 768 word long circular buffers. However, although a 768 word long circular buffer could be defined, in practice, the compiler would allocate a 1024 word long block.

Thus, rather than configuring the shower memories as 768 word long circular buffers, more efficient use of the PLD memory resources was made by partitioning each shower memory into a 256 word long rotating pre-trigger portion and a 512 word long non-rotating post-trigger portion. In practice, this fixed trigger point, $\frac{1}{3}$ of the way through the buffer, has not proven to be a limitation.

4.3. Shower triggers

The PLD continuously monitors the data being loaded into the circulating shower memory buffer, looking for potentially interesting patterns.

As the goal is to push the trigger threshold as low as possible, consistent with manageable trigger rates, it is necessary to consider only the 3 high gain PMT outputs in determining a trigger.

The simplest trigger is based upon the data in a single time bin. Next, one needs to decide how to combine the results of the 3 PMTs. Two variations were possible; either we combine the signals (e.g. add) from the 3 PMTs and then apply a trigger threshold, or we apply a trigger threshold independently to each of the input channels and combine the outputs. We opted to implement both variations at this stage. One can select either, to require that the sum of the pulse heights of a specified subset of the inputs is above a predetermined threshold (sum trigger), or that greater than or equal to a specified number of inputs are above a specified threshold (multiplicity trigger). In either case a subset of inputs may be selected to participate.

In practice, the multiplicity trigger has been found to be more noise resistant, being less sensitive to gain shifts or direct light in a single PMT. Additionally, one can tune the multiplicity trigger to reflect the spatial characteristics of the signals of interest. For example, requiring only 2 of the 3 PMTs to be involved improves the efficiency for triggering on signals which do not contribute equally to the 3 PMTs. As a result, the sum trigger is not used in the array.

The single time bin trigger is effective for narrow signals, where the amplitude of the signal conveys a significant portion of the information. It is not effective, however, for small amplitude signals distributed over many time bins. The former is characteristic of signals in tanks near the shower core, or for signals from steeply inclined showers. The latter is characteristic of the signals of primary interest, signals far from the core of large (not too steeply inclined) showers.

In order to trigger efficiently on these signals, an additional trigger channel was implemented, which incorporates both signal duration and signal amplitude. The first stage of trigger logic for this "time-over-threshold" trigger is identical to that employed in the single bin trigger. The time-over-threshold trigger condition is satisfied when the first stage is active for more than a specified duration, within a sliding window. The length of the window may be specified to be between 1 and 256 time bins, while the required duration may be set to the length of the window. An example of the time-over-threshold trigger timing is shown in Fig. 3.

Figs. 4 and 5 show examples, from the current data stream, of single bin trigger and time-over-threshold triggers. The time-over-threshold trigger has proven to provide the cleanest sample of normal cosmic ray air shower events. Typically, the single bin trigger algorithm now produces a 100 Hz rate at the front end, while the time-over-threshold algorithm produces a few Hz rate.

4.4. Muon memory

Through-going muons provide a natural calibration signal for the detectors. The average integrated single muon signal provides an absolute gain calibration, while the decay time of the muon signal monitors the water clarity and the tank liner reflectivity. (Longer water attenuation length and higher tank wall reflectivity increases the probability that a Cherenkov photon will eventually

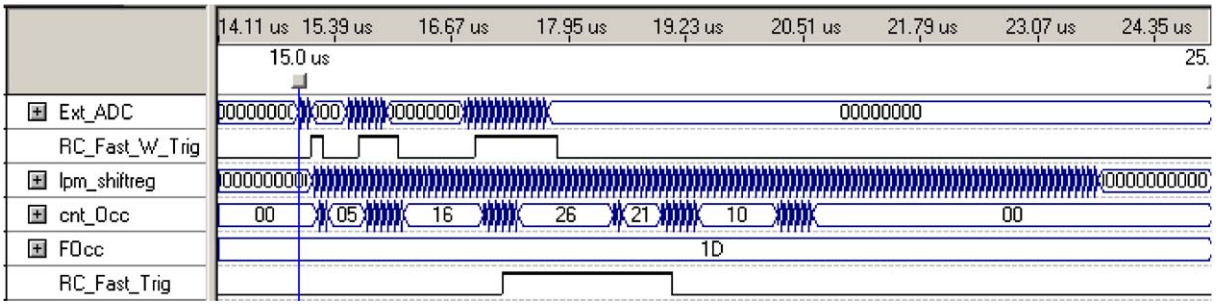

Fig. 3. An example of time-over-threshold trigger simulation. Three input pulses (signal Ext_ADC) generate preliminary triggers (RC_Fast_W_Trig) which propagate in the shift register (lpm_shiftreg). The final trigger (RC_Fast_Trig) is generated when the occupancy (cnt_Occ) is above the required value (FOcc).

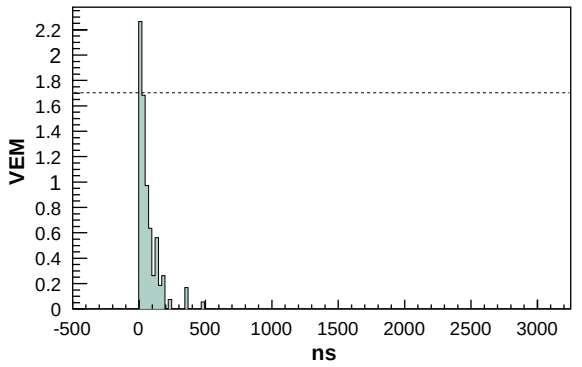

Fig. 4. An example of a signal that generated a single bin trigger. The signal is calibrated in units of "vertical equivalent muons" (VEM). The trigger threshold of 1.7 VEM in each of the high gain PMT channels is indicated by the dashed line. Only 1 of the 3 PMT signals is shown.

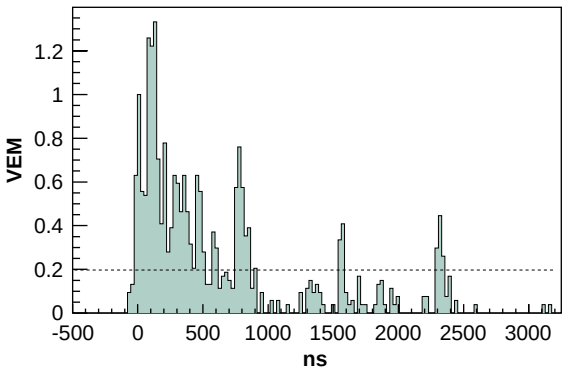

Fig. 5. An example of a signal that generated a time-over-threshold trigger. The signal is calibrated in "vertical equivalent muons" (VEM). The trigger condition is 0.2 VEM in >12 bins in at least 2 of the 3 high gain PMT channels. The threshold is indicated by the dashed line. Only 1 of the 3 PMT signals is shown.

reach a PMT after multiple reflections and a corresponding time delay.)

In order to make effective use of this free calibration source, a large sample of muons needs to be collected in each tank. We therefore implemented muon buffers, optimized to collect large samples of muons.

The muon buffers are stored in the dual port static RAM chip, external to the PLD. The size of the RAM chip allows for two 32-bit wide, 8k word long buffers.

Since the muon signals are relatively narrow (typically 10 ns rise, 70 ns fall), a single time bin trigger is appropriate. And since the signals are relatively small (typically 50 ADC counts above pedestal per PMT at the peak), only the high gain PMT outputs are recorded.

When a signal above threshold (with signal sum and multiplicity options as for the shower trigger) is observed, a time tag and 8 data words (3 pre-trigger and 4 post-trigger) are stored in the muon memory. The time tag is omitted if not necessary (e.g. the data follow immediately after the previous data in time).

A special feature of the muon buffers is a 2nd trigger level, which can be activated for a fixed interval after each trigger. The idea behind this trigger was to enhance the efficiency for triggering

on events in which a muon stops in the tank, and then decays. Unfortunately, this particular trigger feature has not proven to be an effective way to tag those events.

4.5. Station controller interface

The trigger card is implemented as a memory mapped peripheral on the station controller bus. Control operations proceed by accessing memory mapped registers with programmed data transfer operations. No particular effort was expended to make these operations fast, as once configured, few such operations are required during normal data-taking.

The event data readout, however, was optimized for the highest possible speed, consistent with component timing margins. Event data readout proceeded by DMA, using the fly-by-burst DMA mode of the PowerPC, in which data from the trigger circuitry were transferred directly to station controller memory. In the EA, one 32-bit data word was transferred to memory each clock cycle. Subsequently, we have taken a slightly more conservative approach and reduced the transfer rate to one word every 2 clock cycles, in order to improve the timing margins.

5. Code organization

The PLD code is heavily pipelined [8]. In order to keep this in mind, the code modules were organized and named according to the pipeline stage. This is illustrated in Fig. 6.

The pipeline nature of the code also meant that the readout pipeline in the PLD had to be filled prior to starting a DMA operation, in order to avoid stale data appearing at the beginning of each DMA block. This required 5 clock cycles prior to the start of the DMA from shower memory (Fig. 7).

Muon buffer data are transferred directly from the static RAM to the station controller memory.

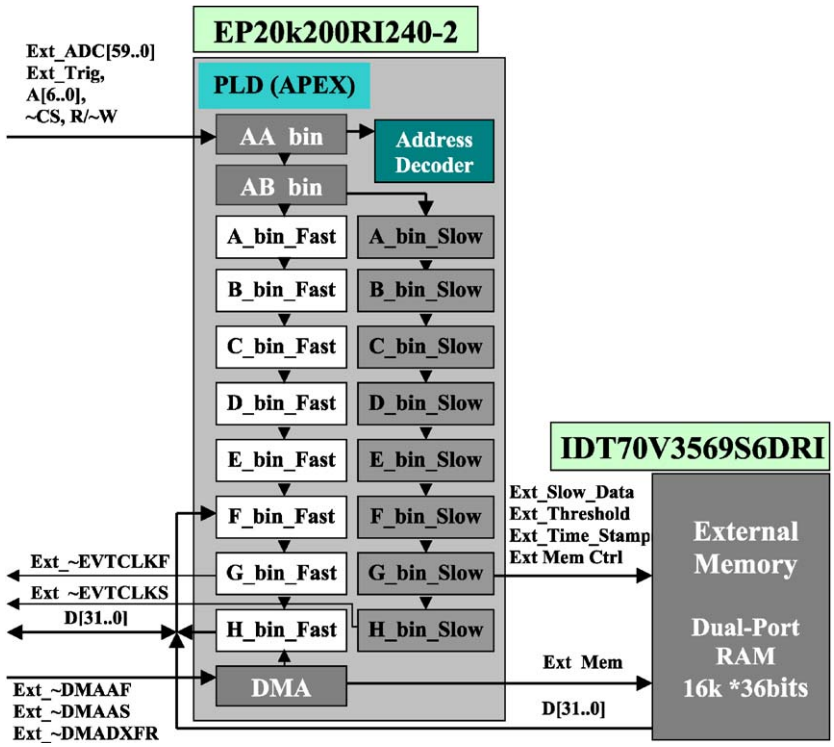

Fig. 6. Pipeline structure of the internal routines.

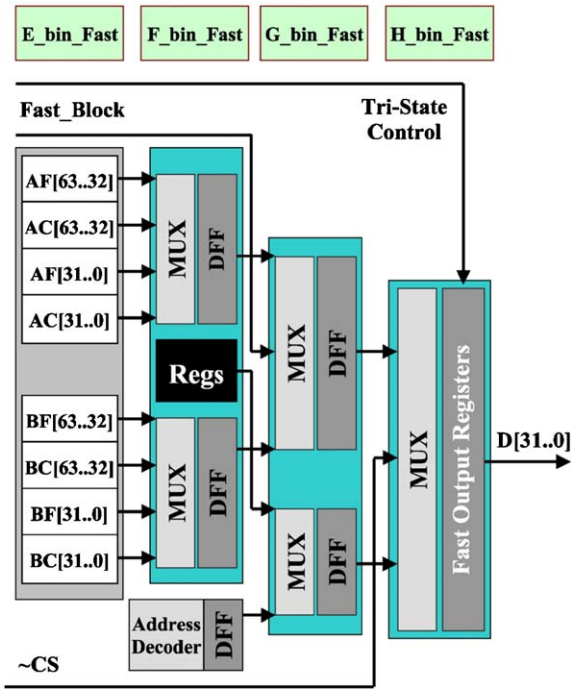

Fig. 7. The structure of the pipeline readout system.

The PLD contains registers in each I/O cell. Careful use of these registers facilitated close synchronization of output data transitions by avoiding variable delays from internal logic cells to the pads.

Each code module implemented a set of operations to partially process the data. For example, the E_bin_Slow routine contains the counter controlling the length of the 2nd trigger level interval, the logic to generate the threshold and time stamp indicators, and the time stamp counter. Actual insertion of the time stamps into the data stream is performed by the next module in the chain, F_bin_Slow.

More details can be found in Refs. [5,6] and the references therein.

6. Power consumption

The PLD requires 2 supply voltages, 3.3 V for I/O and 2.5 V for the core. The power consumption of the chip depends on the internal rate of operations. The power consumption has been measured as a function of trigger rate under simulated operating conditions with a station controller. This is shown in Fig. 8. In actual operating conditions trigger rates were kept below ≈ 100 Hz, and the power consumption of the trigger board was less than 1 W.

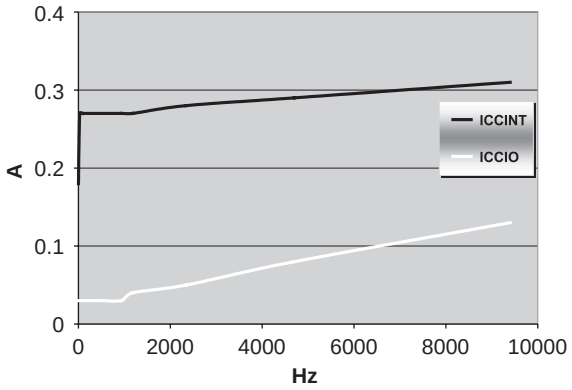

Fig. 8. The measured current consumption as a function of the trigger rate. ICCINT is the current used in the core of the PLD and ICCIO is the current used in the input/output circuits. The jump in the core current near the left axis corresponds to the activation of the circulating buffer during the test.

7. Summary

The trigger/memory circuitry described above was successfully operated in the Auger Observatory Engineering Array. The successful operation in the EA demonstrated the suitability of PLD based trigger logic in the Auger surface detectors, and provided solid practical experience for the subsequent production design [9].

The successful field validation of the simulated performance and laboratory measurements allowed us to switch to lower cost PLDs for the production implementation, confident that simulations and laboratory measurements of the revised design would accurately predict field performance.

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