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Second-level trigger in the Pierre Auger Fluorescence Detector

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Abstract

The development and design of the second-level trigger for Fluorescence Detector in the Pierre Auger Experiment implemented in VLSI Altera FPGA chips is presented. Results show that Altera chip is a very good choice for sophisticated projects ensuring low propagation time, flexibility and sufficient capacity. © 2001 Elsevier Science B.V. All rights reserved.

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Keywords: Pierre Auger observatory; Fluorescence detector; FPGA; VLSI

1. Introduction

The Fluorescence Detector (FD) is one part of the Auger Observatory [1,4]. The atmospheric fluorescence measurements, although only available on clear moonless nights, play an essential role by providing a subset of showers measured both laterally and longitudinally. The primary role of the fluorescence detector is to measure the longitudinal profile of each shower. The FD is built from a set of mirrors with a matrix of PMTs (22×20). Each camera observes a 30° sector of the sky. The task of the second-level trigger is to recognize if the PMT signals from the matrix correspond to a real shower track or to a noise event. Since the experiment is expected to operate for a minimum of 15–20 years, highly reliable electronics as well as flexibility for future modification are required. Programmable logic devices of ultra-high scale integration have both features. The large scale of integration reduces the number of chips, while programmability provides the flexibility and reduces the cost of prototypes and final designs. A standard technique for noise reduction is the implementation of coincidences of sufficient order. A compromise between signal-to-noise ratio and efficiency has to be achieved.

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2. Four-fold coincidences only

The Fluorescence Detector built from a set of cameras with a matrix of PMTs collects light produced from nitrogen fluorescence activated by

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ultra-relativistic showers in the atmosphere. Each camera of the FD contains 440 hexagonal PMTs. The observation angle of each PMT is relatively narrow, only 1.5°. Such fine angular resolution leads to a narrow track image on the PMT surface, often below the transversal size of PMT. A group of PMT signals generated by a real track forms collinear patterns only. Discriminator circuits compare each PMT signal to a first-level trigger (FLT) threshold and produce "pixel fired" signals for above threshold inputs. These signals form the elements of the sought collinear patterns. The main trigger will be generated on the bases of a set of collinear patterns; however, even collinear patterns may be generated by sky background, point sources like aircraft as well as by random electronic noise. Nevertheless, the probability of accidental coincidences is small if an appropriate coincidence level is chosen. A general calculation assuming uncorrelated inputs shows that the 4-fold level is sufficient. The trigger and readout system is implemented in one PLD chip to achieve speed, flexibility, reliability and the option to make substantial changes to the algorithm on line. All of the above criteria are met in a cost-effective solution with the Altera FLEX10k family. To estimate the capacity and flexibility of the 10k family, the configuration files for triggers of 4-fold "collinear" coincidences have been prepared for rectangular and hexagonal matrices of various sizes [2,3]. Results show the second-level trigger can be built in all cases from a single chip with propagation times less than 100 ns (see Fig. 1). In each case, the minimal size of the chips, which can contain the circuit, is listed in Table 1.

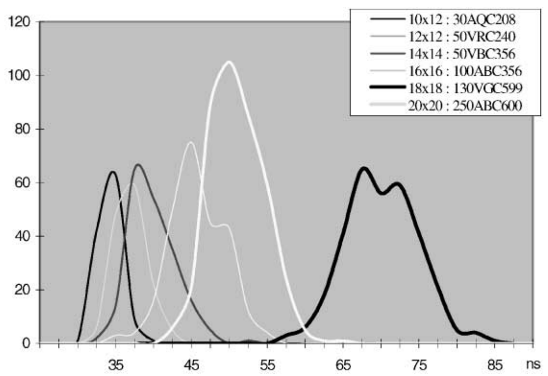


Fig. 1. Distribution of propagation time for 4-fold "continuous" coincidences.

The prototype of the trigger for a 10×12 matrix has been built and tested at the University of Lodz. All 120 inputs could be driven simultaneously. For a 22×20 matrix simultaneous connection of all 440 I/O pins to the trigger is difficult due to a huge number of inputs. Thus, for the implementation of the second-level trigger a multiplexing technique has been chosen. In this design the full PMT matrix will be sequenced through a "scanning window" where a subset of the pixels is examined at each step.

3. A tabulation of the patterns and 4-fold coincidences

If the light falling on a PMT is under the threshold, a gap or missing end point will occur on the track. As a consequence, the requirement of a 5-fold coincidence would result in unacceptable efficiency for the showers of interest. However,

Table 1
The minimal size of the chips with the number of terms and used logic cells needed to implement second-level trigger with "continuous" 4-fold coincidences for rectangular and hexagonal matrices

Size	No. of terms	Rectangular	Logic cells	No. of terms	Hexagonal	Logic cells
10×12	2456	30AQC208	1458 (84%)	1703	30AQC208	969 (56%)
12×12	3086	50VRC240	1913 (66%)	2132	30AQC208	1260 (72%)
14×14	4474	50VBC356	2799 (97%)	3065	50VBC356	1911 (66%)
16×16	6118	100ABC356	3842 (76%)	4166	50VBC356	2585 (89%)
18×18	8018	130VGC599	5455 (81%)	5435	70VGC503	3503 (93%)
20×20	10174	250ABC600	6488 (53%)	6872	130VBC600	4559 (68%)
22×20	11316	250ABC600	7201 (59%)	7628	130VBC600	5013 (75%)

since 4-fold coincidences reduce sufficiently the noise, they will be incorporated in the trigger. Such 4-fold patterns created by the removal of one PMT from 5-fold patterns will be processed by the 4-fold logic chosen. In all cases a pattern is characterized by the horizontal and vertical indices of the pixels whose signals are sensed above the threshold. The first step in specifying the trigger is a determination of the complete set of indices (4 pairs) that are to be presented to 4-fold coincidence logic.

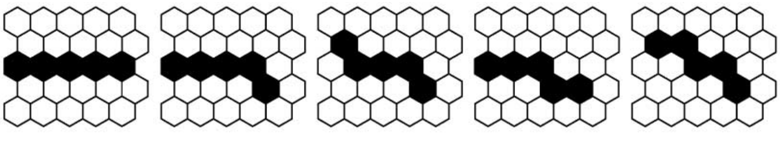
The five topologically different 5-fold patterns are:

- 5 PMTs in a single row (5).
- One PMT deflected from the main direction (4–1)
- Two PMTs deflected from the main direction from both ends (1–3–1).
- 3 PMTs lying on one row and the next two on the neighboring one (3–2).
- PMTs lying on three neighboring rows $2+2+1$, respectively (2–2–1).

All patterns that can be obtained from the basic patterns by horizontal or vertical translation must be included and tabulated. Patterns obtained by mirror reflection or by rotation, taking into consideration the 60° geometry are then added to the list. In all, 39 different basic patterns remain. This count doubles as a result of the hexagonal matrix, which has 60° symmetry. In this geometry the indices of PMTs lying in odd and even rows cannot be obtained directly by vertical shifting. The patterns for even and odd vertical indices have to be taken into consideration separately. Thus, the basic pattern count (called classes) increases to $2*39 = 78$.

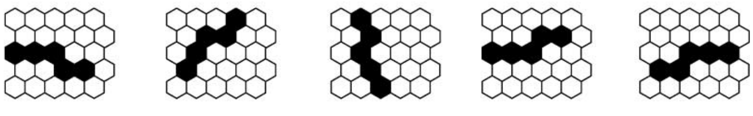
Finally, a list of all 4-pixel indices (the numbers that defined the inputs to the coincidence circuit) that result from patterns and location is generated. This list of 4-fold coincidence indices contains duplicates when the remaining 4 tubes from 2 distinct patterns are the same after one tube is removed. These duplicate coincidences are then removed. The 78 basic patterns (classes) expand to 390 4-fold coincidences which, in turn, reduces to 271 when duplicates are removed (see Figs. 2–5 and Table 2).

A minimal width of the scanning window is five columns and corresponds to the 5-fold coincidence. For a scanning window, the total number of patterns is **7392**. Nevertheless, not all are independent. Some of the patterns come from different parents, but have the same set of indices. Such repeated patterns are removed. The number of non-repeated patterns decreases to **5633**. Some of the classes consist entirely of removed patterns, causing the number of classes to be reduced. Only **216** classes survived.



5	4_1	1_3_1	3_2	2_2_1

Fig. 2. Types of topologically different 5-fold patterns.



Basic pattern	60° rotated	120° rotated	X-axis mirrored	Y-axis mirrored

Fig. 3. Symmetry transformation of basic pattern.

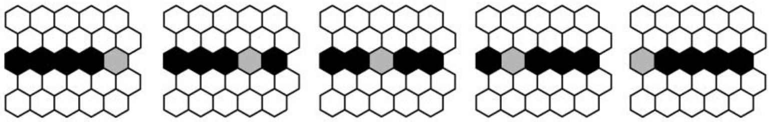


Fig. 4. A construction of patterns with gap.

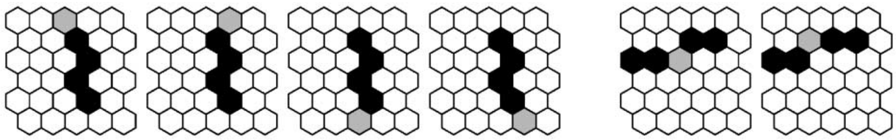


Fig. 5. Samples of patterns with the same set of indices, but coming from different parents.

Table 2
The set of indices for basic 5-fold patterns

	Patterns[a]	Y 1	X 1	Y 2	X 2	Y 3	X 3	Y 4	X 4	Y 5	X 5
1	N5_0	1	1	1	2	1	3	1	4	1	5
2	P5_0	2	1	2	2	2	3	2	4	2	5
3	N5_60	5	1	4	1	3	2	2	2	1	3
4	P5_60	6	1	5	2	4	2	3	3	2	3
5	N5_120	1	1	2	1	3	2	4	2	5	3
6	P5_120	2	1	3	2	4	2	5	3	6	3
7	N41UR0	2	1	2	2	2	3	2	4	1	5
8	P41UR0	3	1	3	2	3	3	3	4	2	4
9	N41UR60	5	1	4	1	3	2	2	2	1	2
10	P41UR60	6	1	5	2	4	2	3	3	2	2
11	N41UR120	1	1	1	2	2	2	3	3	4	3
12	P41UR120	2	1	2	2	3	3	4	3	5	4
13	N41UL0	1	1	2	1	2	2	2	3	2	4
14	P41UL0	2	1	3	2	3	3	3	4	3	5
15	N41UL60	4	1	4	2	3	3	2	3	1	4
16	P41UL60	5	1	5	2	4	2	3	3	2	3
17	N41UL120	1	1	2	1	3	2	4	2	5	2
18	P41UL120	2	1	3	2	4	2	5	3	6	2
19	N41DR0	1	1	1	2	1	3	1	4	2	4
20	P41DR0	2	1	2	2	2	3	2	4	3	5
21	N41DR60	4	1	3	2	2	2	1	3	1	4
22	P41DR60	5	1	4	1	3	2	2	2	2	3
23	N41DR120	1	2	2	1	3	2	4	2	5	3
24	P41DR120	2	1	3	1	4	1	5	2	6	2
25	N41DL0	2	1	1	2	1	3	1	4	1	5
26	P41DL0	3	1	2	1	2	2	2	3	2	4
27	N41DL60	1	3	2	2	3	2	4	1	5	2
28	P41DL60	2	2	3	2	4	1	5	1	6	1
29	N41DL120	1	1	2	1	3	2	4	2	4	3
30	P41DL120	2	1	3	2	4	2	5	3	5	4

Table 2 (*continued*)

	Patterns[a]	Y 1	X 1	Y 2	X 2	Y 3	X 3	Y 4	X 4	Y 5	X 5
31	N131P0	3	1	2	1	2	2	2	3	1	4
32	P131P0	4	1	3	2	3	3	3	4	2	4
33	N131P60	1	2	2	2	3	2	4	1	5	2
34	P131P60	2	1	3	2	4	1	5	1	6	1
35	N131P120	1	1	1	2	2	2	3	3	3	4
36	P131P120	2	1	2	2	3	3	4	3	4	4
37	N131N0	1	1	2	1	2	2	2	3	3	4
38	P131N0	2	1	3	2	3	3	3	4	4	4
39	N131N60	3	1	3	2	2	2	1	3	1	4
40	P131N60	4	1	4	2	3	3	2	3	2	4
41	N131N120	1	2	2	1	3	2	4	2	5	2
42	P131N120	2	1	3	1	4	1	5	2	6	1
43	N32UR0	2	1	2	2	2	3	1	4	1	5
44	P32UR0	3	1	3	2	3	3	2	3	2	4
45	N32UR60	5	1	4	1	3	2	2	1	1	2
46	P32UR60	6	1	5	2	4	2	3	2	2	2
47	N32UR120	1	1	2	1	2	2	3	3	4	3
48	P32UR120	2	1	3	2	3	3	4	3	5	4
49	N32UL0	1	1	1	2	2	2	2	3	2	4
50	P32UL0	2	1	2	2	3	3	3	4	3	5
51	N32UL60	4	1	3	2	3	3	2	3	1	4
52	P32UL60	5	1	4	1	4	2	3	3	2	3
53	N32UL120	1	1	2	1	3	2	4	1	5	2
54	P32UL120	2	1	3	2	4	2	5	2	6	2
55	N32DR0	1	1	1	2	1	3	2	3	2	4
56	P32DR0	2	1	2	2	2	3	3	4	3	5
57	N32DR60	4	1	3	2	2	2	2	3	1	4
58	P32DR60	5	1	4	1	3	2	3	3	2	3
59	N32DR120	1	1	2	1	3	1	4	1	5	2
60	P32DR120	2	1	3	2	4	1	5	2	6	2
61	N32DL0	2	1	2	2	1	3	1	4	1	5
62	P32DL0	3	1	3	2	2	2	2	3	2	4
63	N32DL60	1	2	2	1	3	1	4	1	5	1
64	P32DL60	2	2	3	2	4	1	5	2	6	1
65	N32DL120	1	1	2	1	3	2	3	3	4	3
66	P32DL120	2	1	3	2	4	2	4	3	5	4
67	N221R30	3	1	2	1	2	2	1	3	1	4
68	P221R30	4	1	3	2	3	3	2	3	2	4
69	N221R90	1	2	2	1	3	2	4	1	5	2
70	P221R90	2	1	3	1	4	1	5	1	6	1
71	N221R150	1	1	2	1	2	2	3	3	3	4
72	P221R150	2	1	3	2	3	3	4	3	4	4
73	N221L30	3	1	3	2	2	2	2	3	1	4
74	P221L30	4	1	4	2	3	3	3	4	2	4
75	N221L90	1	1	2	1	3	1	4	1	5	1
76	P221L90	2	1	3	2	4	1	5	2	6	1
77	N221L150	1	1	1	2	2	2	2	3	3	4
78	P221L150	2	1	2	2	3	3	3	4	4	4

[a] N, P: correspond to odd and even vertical indices, respectively; 5, 41, 131, 32, 221: correspond to topological type of pattern; UL, UR, DR, DL and N, P: subclasses in 41, 32 and 131, 221 classes, respectively; 0, 60,120, 30, 90, 150: rotation angles of basic pattern.

4. Scanning of matrix

Scanning of the 22×20 matrix will be performed in 10 steps. In each step, two columns of 44 pixel triggers are read every 100 ns. Previously read columns are shifted in shift registers. For 10-step scanning, the minimal width of a scanning window should be 6 columns. A simultaneous analysis of whole patterns in the scanning window (22×6) would correspond to **7735** non-repeated ones. However, it is sufficient to take into consideration patterns starting from the 1st and 2nd columns only. Patterns starting from the next columns will be analyzed in the next scan. This reduces the number of simultaneous analyzing patterns to **4204** only. The transfer frequency from pixel trigger to second-level trigger is set to 10 MHz. However, to reduce the number of simultaneous analyzing patterns, the scan frequency can be increased internally to 20 MHz (loading of data as previously 10 MHz, but with internal buffer added) then the analysis can be limited to the patterns starting from the 1st column only (scanning window 22×5). The number of simul-

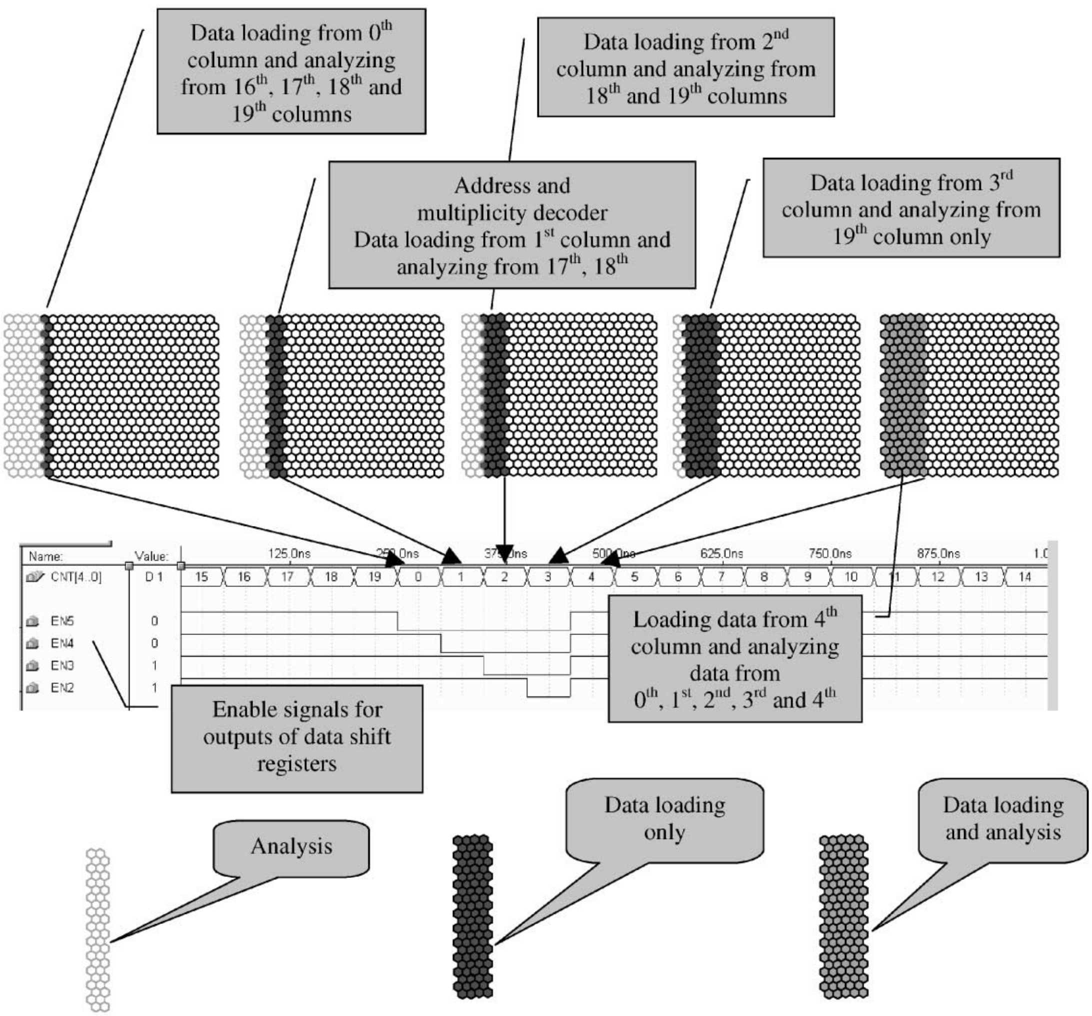


Fig. 6. The scheme of data analysis when the scanning window starts the new scans.

taneously considered patterns can be reduced to **2102**. Such an approach allows the use of a smaller and cheaper chip.

Data from pixel triggers are loaded (at 10 MHz) to local storage registers (P0 and P1) and multiplexed at 20 MHz to 5-stage shift registers (D5–D1). If the 22×5 window scans columns from 4th to 19th data from outputs of all shift registers are given onto the matrix recognizing **2102** patterns (E block). When the scanning window reaches the end of PMT matrix and starts the new scanning cycle, data from the 0th column are only loaded, but data from the previous cycle (from the 16th to 19th column) are still being analyzed. In the next steps, data from FLT are progressively loaded but the 1st, 2nd and 3rd columns are progressively disabled to prevent an analysis from columns 17–19, 18–19 and finally 19 only, respectively. Possible patterns that combined partially from the beginning and the end of the matrix do not correspond to the real track and have to be rejected by disabling the appropriate output of shift registers according to Fig. 6.

5. "Angle" classes

Each of the surviving classes corresponds to a specific range of track angles. Additional nodes inside the chip are used to indicate the angular region of registered patterns. Patterns are first grouped (as a logical sum) into **216** surviving classes and next into classes corresponding to the angle of fitted line of the fired PMTs. The patterns in two surviving classes which can be covered themselves by vertical shift have the same angular origin. Hence, the number of independent angular classes reduces twice to **108** only.

Let us find the angle of the line, which fits the geometrical centers of "fired" PMTs. Although the signals over the thresholds in each PMT may be different, this corresponds to a different light energy transferring into PMTs and different angle of a real track, the best fit for "fired" pattern will be fixed. Therefore, we can only obtain approximate angular region but by hardware this can be done very fast. The distribution of fitted angles is not continuous.

The angles given by the hardware should be treated as the first estimate only. As seen from Fig. 7, not all angles are represented. The angle gaps correspond to the quantified pattern structures. The next step in angle analysis takes into consideration weights from FADCs. After such fitting, the distribution of angles will be continuous.

The normal line equation is given by

$$x \cos \alpha + y \sin \alpha - p = 0$$

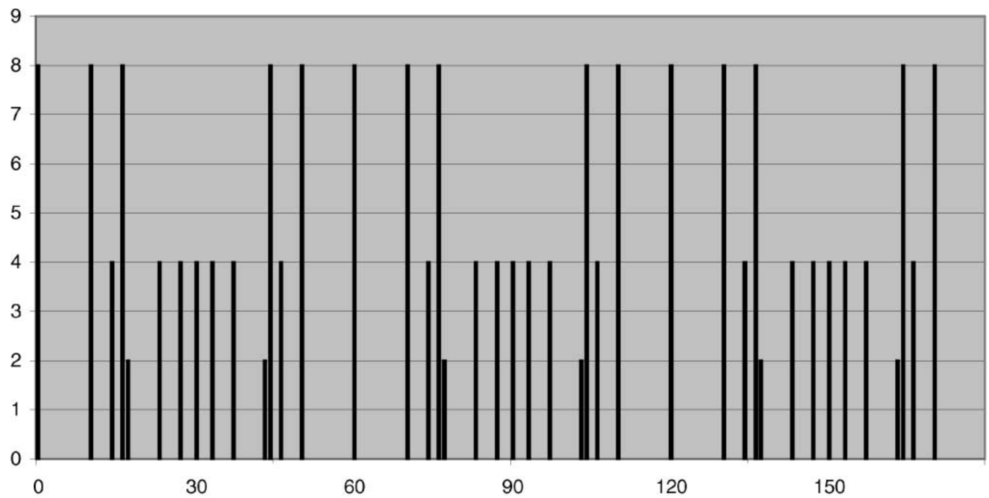


Fig. 7. The distribution of the surviving classes angles.

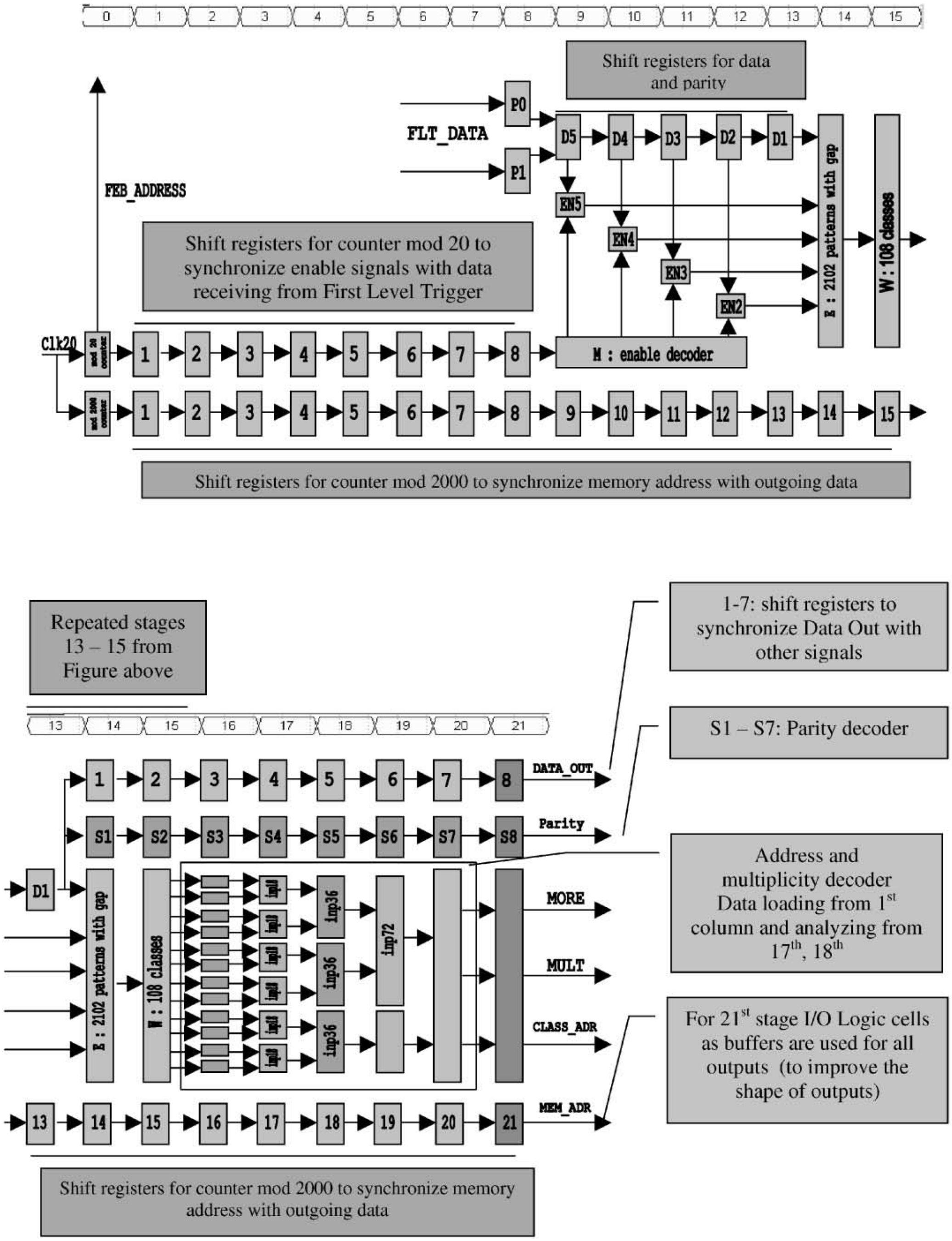


Fig. 8. Design of the internal structure of second-level trigger.

where α is the angle between line and X-axis and p is the distance from the line to the beginning of coordinate system and x, y are points on line.

Let us minimize the sum of the square distance of PMT centers from fitting line

$$\sigma = \sum_{i=1}^{n} (x_i \cos\alpha + y_i \sin\alpha - p)^2.$$

The fitted angle of line is as follows:

$$\tan 2\alpha = 2 * \frac{(1/n)S_x S_y - S_{xy}}{S_{yy} - S_{xx} + (1/n)(S_x^2 - S_y^2)}$$

where n is the number of fitted points and S_{xx}, S_{yy}, S_{xy}, S_x, S_y are described below;

$$S_{xx} = \sum_{i=1}^{n} x_i^2 \quad S_{yy} = \sum_{i=1}^{n} y_i^2 \quad S_{xy} = \sum_{i=1}^{n} x_i y_i$$

$$S_x = \sum_{i=1}^{n} x_i \quad S_y = \sum_{i=1}^{n} y_i.$$

The distribution of the surviving class angles is shown in Fig. 7.

6. General design

The scheme of the second-level trigger implemented in an Altera chip is given in Fig. 8. Each 4-fold coincidence defines an angle "class" based on the average angle of tracks producing the pattern in addition to generating a trigger signal, MULT. This overall trigger signal initiates the reading of the entire 22×20 PMTs matrix. To improve the processing speed, the design includes pipeline stages. This approach helps to eliminate glitches at the expense of a modest increase in component resources within the chip. An additional output, MORE, indicates an event where two or more angle classes are active at the same time. In this case, the unique angular class number cannot be generated.

Second-level trigger sends the address to front end boards (10 channels per 44 pixel triggers) and after 6 clock cycles (20 MHz) receives data. To synchronize data written to the external memory, the FEB address is shifted in the shift register chain. The reduction, simultaneously considering patterns to **2102**, allowed decreasing the propagation time below 1 clock cycle (50 ns). Therefore, the 14th step corresponds to parallel 2102 four-input AND gates. The generation of "angle" classes from 2102 patterns to 108 ones requires relatively simple logic, which can be implemented in one time bin (15th). However, obtaining binary address from the set of 108 outputs of "angle" classes requires much more complicated logic, which has been developed in cascade chain (16 to 20th time bins) in several parallel blocks. Coder blocks are the same in the 16 to 18th time bins, respectively. In the 19 and 20th time bins work 3 combinational decoders generating binary "angle" class address, when only one output in W block is active (1 from 108). Additionally, S1–S7 blocks form the pipelined parity decoder indicating possible data deformation.

7. Conclusion

All electronics described above have been implemented into one Altera chip of the fastest version (suffix-1). The smallest version with sufficient capacity is EPF10k100ARC240-1 (quad flat package) with 88% of the logic cells used. The timing analyzer shows that the registered performance for this version is sufficient to run the trigger at 40 MHz internally. At this speed, data from FLT could be loaded with 20 MHz and a full scan could be decreased from 1000 to 500 ns.

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